REMARKS

The application contains claims 1-7 and 9-27. Claims 20-27 are new. In view of the foregoing amendments and following remarks, Applicants request allowance of the application.

The objections noted in paragraphs 1 and 2 of the Office Action have been overcome. Specifically, the legend "Prior Art" has been added to FIG. 1 and the recommended specification corrections have been adopted.

Claim 4 has been amended to recite subject matter of dependent claim 8, which the Office Action identifies as reciting allowable subject matter. Claim 4 and dependent claims 5-7 are allowable. Amendments to claims 6 and 7 have been entered to maintain consistency in terminology; they have nothing to do with patentability.

CLAIMS 1-3 SATISFY 35 U.S.C. § 101

Applicants respectfully request withdrawal of the § 101 rejection to claims 1-3 because the claims define statutory subject matter. Applicant respectfully notes that the guidelines for computer implemented inventions provided in MPEP 2106. For a claim to define statutory subject matter, it need only recite subject matter that is useful, concrete and tangible. AT&T Corp. v. Excel Communications. Inc., 172 F.3d 1352 (Fed. Cir. 1999). The pending claims satisfy this requirement.

Traces are units of program instructions that are assembled in program order. They certainly are concrete and tangible; they can be stored in memories, such as the block cache 280 of FIG. 2, retrieved from memory and executed. They also are useful. The specification at pp. 2-3 and elsewhere lists several performance advantages that the claimed invention provides over other types of traces that were available in the prior art. Accordingly, the claimed subject matter meets every requirement announced by the Federal Circuit for statutory subject matter.

Note also that the claimed subject matter satisfies § 101 under the older analysis described in MPEP 2106 and cited in the Office Action. The traces of claims 1-3 should be considered functional descriptive subject material because they describe a data structure that imparts functionality when employed within a processor. As described by the specification, the multiple entry, single exit structure has several advantages over other approaches. For

example, it can eliminate instruction redundancies within a cache and lead to improved efficiencies therein. Just like other data structures, the traces of the pending claims are drawn to statutory subject matter.

Claims 1-3 satisfy the requirements of 35 U.S.C. § 101. Applicants respectfully request that the rejections on this ground be withdrawn.

CLAIMS 13 AND 9-19 ARE ALLOWABLE OVER THE CITED ART.

Claims 1-3: Arbabi is not Directed to Any Type of Trace

Arbabi has almost nothing to do with claims 1-3. Claim 1 defines a ***trace*** having a multiple entry, single exit architecture. Arbabi shows a drawing (FIG. 9) having such a structure but his disclosure relates to neural networks ***not traces***. A trace is a well known concept in processor architectures; it refers to a collection of program instructions that are assembled into a unit according to a predetermined scheme based on program order. Although the Office Action acknowledges as much in its § 101 analysis, it disregards this when considering the claim in the context of prior art. Respectfully, this is improper.

Arbabi's neural network is composed of a number of nodes, each of which receives weighted input data from a variety of sources and generates an output. No reasonable reading of this reference can lead one of skill in the art to conclude that Arbabi discloses any form of trace. Claims 1-3, therefore, define over this reference and the anticipation rejection should be withdrawn.

Claims 9-15 Define Over Black

Claim 9 stands rejected as anticipated by Black, "The Block-Based Trace Cache." Applicants respectfully request withdrawal of this rejection because Black does not teach or suggest all elements of the claim. For example, claim 9 recites:

> predicting an ***address of a terminal instruction*** of an extended block to be used,
> determining whether the predicted address matches an address of a ***terminal instruction*** of a previously created extended block, and

Black does not teach or suggest this subject matter. The Office Action identifies the trace_ID (FIG. 2) as representing a predicted trace but Black does not disclose that this trace is an address of a terminal instruction within the trace. In § 5.4, Black states that the trace_ID is the concatenation of the last block_ID, the last 3 branch directions and the block_ID fetched 3 blocks earlier. Any address associated with an internal instruction has no relevance to the trace_ID. Thus, claim 9 defines over Black. Claims 9-15 are allowable over this art.

Claims 16-19 Define Over Black

Claim 16 also stands rejected as anticipated by Black. Claim 16 now recites:

> a front end stage to store blocks of instructions in a multiple-entry, single exit architecture when considered according to program flow, and

Black does not teach or suggest this subject matter. In the Office Action's analysis of claim 6, it asserted that Black taught a single-entry, multiple-exit architecture through use of a replicated block cache and a final collapse processing stage. This disclosure, however, describes Black's processing system not his traces. As recited in claim 16, the multiple-entry, single exit architecture refers to the ***blocks of instructions***. Black traces are not disclosed as having the required structure. Therefore, independent claim 16 is allowable over the cited art, as well as claims 17-19.

NEW CLAIMS 20-27

New claims 20-27 are presented for examination. These claims recite the multiple entry, single exit architecture of the pending claims in other ways. Claim 23 recites that a trace is indexed using an address of a last instruction therein. These claims also are believed to be allowable over the cited art.

Allowance is solicited.

Respectfully submitted,

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